Patent Application of

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for

Adaptive Slope Compensator for Current Mode Power Converter

Field of Invention

This invention relates to the power converters and more specifically to current mode power converters.

Background of the Invention

Various power converters are presently ~~converter are~~ available for transforming ~~an~~ unregulated input voltage to a regulated output voltage with a specific magnitude. Various ~~The technologies of~~ power conversion techniques such as forward and flyback are well described as the prior art. Although the advantages of current mode control over voltage mode control has been amply demonstrated, ~~the~~ slope compensation must generally ~~has to~~ be added in the current loop to solve ~~the~~ instability problems. Many texts ~~can~~ explain the operation of current mode and the required slope compensation, such as (a) Keith H. Billings " Switchmode Power Supply Handbook" McGraw-Hill Book Co., p3.148-p3.150 (b) Abraham I. Pressman " Switching Power Supply Design" McGraw-Hill Book Co., p105-p136 ; p143-p165. (c) Modelling, Analysis and Compensation of the Current-Mode Converter" Unitrode Corp. Application Note U-97 (d) "Practical Considerations in Current Mode Power Supplies" Unitrode Corp. Application Note U-111. However, there still exist several drawbacks in conventional ~~slope compensation technologies. Thus, in order to solve the problem and improve the~~ performance, mathematical analysis and practical circuit tests ~~test~~ have been performed to establish the fundamentals of this invention. The characteristic analysis of conventional slope compensation are listed as follows,

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(**A**) Advantage I : Slope compensation stabilizes ~~stabilize~~ the current loop

A general circuit of a conventional current mode power converter is shown in **Fig. 1**, and its symbols defined are :

Pwr: power converter
N_P: primary turn ratio of T_M
L_P: primary inductance of T_M
I_P: primary current of T_M
I_{PA}: primary average current of T_M
I_{SP}: secondary peak current of T_M
T: switching period of Pwr
T_{OFF}: turn-off time of T
V_{IN}: input voltage of Pwr
Verr: output voltage of the error amplifier
V_{RP}: sensed voltage of resistor R_P
T_M: power transformer
N_S: secondary turn ratio of T_M
L_S: secondary inductance of T_M
I_{PP}: primary peak current of T_M
I_S: secondary current of T_M
I_{SA}: secondary average current of T_M
T_{ON}: turn-on time of T
V_O: output voltage of Pwr
V_{SL}: voltage of slope compensation signal

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There are two distinctly different operating modes of power converters, discontinuous mode and continuous. When ~~If a~~ higher power conversion efficiency is concerned, the continuous mode is much more widely used than the discontinuous mode. The purpose of the following analysis is to determine ~~figure out~~ the criterion for ~~of~~ stabilizing the current loop in which a minimum magnitude of the slope compensation has to be added, if the power converter is operating in *continuous current mode* or if the duty cycle of the power converter is greater than 50 percent. Slope m is the down slope ; $m = dIs / dt = Vo / Ls$. **Fig. 2** shows the continuous mode current waveform, Ip and Is. $I_{SA} = I_{SP} - (dIs/2) = I_{SP} - (m/2) \cdot dt$; $I_{SA} = I_{SP} - (m/2) \cdot T_{OFF}$; $I_{SP} = I_{SA} + (m/2) \cdot (T - T_{ON})$. The peak voltage V_{RP} across the primary current-sensing resistor R_P is $V_{RP} = I_{PP} \cdot R_P = I_{SP} \cdot (Ns/Np) \cdot R_P = [\, I_{SA} + (m/2) \cdot (T - T_{ON})\,] \cdot Ns/Np) \cdot R_P$. Adding the slope compensation to V_{RP}, this feedback signal is stated as $V_C = V_{RP} + (V_{SL}/T) \cdot \Delta T = V_{RP} + (V_{SL}/T) \cdot (\Delta T_{ON} + \Delta T_{OFF})$;

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$$V_C = \frac{Ns}{Np} R_P I_{SA} + \frac{Ns}{Np} R_P \frac{mT}{2} + \Delta T_{ON}\left(\frac{V_{SL}}{T} - \frac{Ns}{Np} R_P \frac{m}{2}\right) + \Delta T_{OFF} \frac{V_{SL}}{T} \qquad (1)$$

Since an amount of energy delivered in a time period T represents power , at the end of one period, power drawn from V_{IN} is $P = L_P I_P{}^2 / (2T) = [L_P \cdot (I_{PP}{}^2 - I_{PA}{}^2)] / (2T)$. But $I_{PP} = I_{PA} + \Delta I_P = I_{PA} + (V_{IN}/L_P) \cdot \Delta T$, ~~Then~~ and thus

T31X
$$P = \frac{1}{2TL_P}(V_{IN}{}^2 . T_{ON}{}^2) + V_{IN}. I_{PA} \frac{T_{ON}}{T} \qquad (2)$$

The current I_{PA} is an energy which cannot ~~energy can not~~ completely delivery to the load during the off time (T_{OFF}) ~~time~~ and still remain~~ing~~ in the transformer. Thus the magnitude of the current I_{PA} is related to the T_{OFF} and T_{ON}. It is easily verified from equation (2), that the feedback loop regulates the output of power converter by controlling T_{ON} . The output voltage Vo is sensed and compared to a reference voltage in the error amplifier (EA). The amplified error voltage Verr (voltage loop signal) is fed to a voltage comparator and compared ~~compare~~ with the Vc (current loop signal). As shown in **Fig. 1**, the on time starts at the clock pulse of oscillator (osc) and ends when the Vc ramp equals ~~to~~ the level of ~~the~~ Verr, thereby the adjustment of T_{ON} is proportional ~~in proportion~~ to the magnitude of voltage Vc and Verr. Mathematically the relationship between Vc and T_{ON} is $\partial V_C / \partial T_{ON} \geq 0$. The deviation from equation (1) can be stated as

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$$\frac{\partial V_C}{\partial T_{ON}} = \frac{V_{SL}}{T} - \frac{Ns}{Np} R_P \frac{m}{2}$$

This can be seen quantitatively as

T33X
$$\frac{V_{SL}}{T} \geq \frac{Ns}{Np} R_P \frac{m}{2} \qquad (3)$$

If the change of T_{ON} is not ~~out of~~ proportional to the Vc , $\partial V_C / \partial T_{ON} < 0$, then the feedback loop will ~~non linearly~~ oscillate non-linearly. Thus the criterion of equation (3) must be satisfied to insure ~~the~~ loop stability ~~stable~~.

(**B**) Advantage II : Slope compensation improves the linearity of the current loop

Before adding the slope compensation, the signal Vc is equal to V_{RP} :

T40X

$$\Delta I_P = \frac{V_{IN}}{Lp} . \Delta T \qquad (4)$$

$$V_{RP} = (I_{PA} + \frac{V_{IN}}{Lp} \Delta T_{ON}).R_P \qquad (5)$$

Equations ~~This is seen from equation~~ (2), (4), and (5), demonstrate that when the output power remains constant, the T_{ON} increases and ΔI_P decreases as V_{IN} goes down. The current waveform corresponding to the V_{IN} and T_{ON} is shown in **Fig. 3** . The current feedback loop signal compared ~~compare~~ with the voltage feedback loop signal will control the output power and regulate the output voltage. It ~~it~~ is obvious the control loop will lose ~~the~~ linearity and ~~noise~~ immunity to noise as V_{IN} goes down. This disadvantage can be improved by adding the slope compensation.

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$$V_C = V_{RP} + \frac{V_{SL}}{T} (\Delta\ T_{ON} + \Delta T_{OFF})$$

$$= I_{PA}.R_P + \frac{V_{SL}}{T} \Delta T_{OFF} + \Delta T_{ON} (\frac{V_{IN}}{Lp}.R_P + \frac{V_{SL}}{T}) \qquad (6)$$

The slope compensation element remains a minimum linearity of the control loop.

(C) Disadvantage I : A dummy load or the minimum load is required to avoid the unstable oscillation during ~~while~~ no load or light load conditions

The conventional ~~current~~ mode power converter ~~per se are known, it~~ will operate in discontinuous mode while the output is in no load or light load conditions and ~~it~~ may operate in continuous mode while the output power is high or the input voltage is low. A minimum magnitude of slope compensation must be added as equation (3), as long as the power converter operates ~~it may operate~~ in the continuous mode. While the power converter is operating in discontinuous mode, its slope compensation included current feedback loop signal Vc is

T42X

$$V_C = \frac{V_{IN}}{Lp}.R_P. \Delta T_{ON} + \frac{V_{SL}}{T} (\Delta\ T_{ON} + \Delta T_{OFF}) \qquad (7)$$

This ~~this~~ signal waveform is shown in **Fig. 4**, illustrating ~~It illustrates the mechanism of~~ a nonlinear deviation in the power control. If the signal Verr goes down due to the regulation, its voltage move from *point C* to *point A* or *point B* will cause a nonlinear deviation. Since the voltage level of *point A* is equal to *point B*, but the on time (T_{ON}) of *point A* and *point B* is different, ~~The~~ difference is (T_{ONB}-T_{ONA}) ~~which~~ causes a deviation P_d in the power control.

T43X

$$P_d = \frac{V_{IN}^{\ 2}}{2TLp} (T_{ONB}^{\ 2} - T_{ONA}^{\ 2}) \qquad (8)$$

Because of this, ~~the effect is then~~ an oscillation ~~which~~ commences at every change in signal Verr ~~and~~ which may continue for some time. Two conventional approaches for solving ~~approach to solve~~ this problem are (a) To equip with a dummy load in the output. This yield $[I_P \cdot R_P > (V_{SL}/T)]$ during the no load or light conditions. However this will consume the ~~a~~ power of the dummy load. (b) To require consuming a minimum power in the load. However, ~~however~~ this cannot ~~can not~~ meet the requirements of ~~the~~ power management. The goal ~~embodiment~~ of power management is to manage the system to only consume ~~only consuming the~~ power during the operation such that ~~And no~~ no power, or little ~~few~~ power is consumed during the non-operation (sleep mode). With

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respect to the power converter in a power management application, ~~how to save~~ conserving the power in the no load or light load conditions is a major requirement.

(D) Disadvantage II : Less than ideal line voltage regulation

Consider how the power converter regulates against line voltage changes. As V_{IN} goes up, the Vo will eventually go up. Then after a delay in getting through the voltage feedback loop , Verr will ~~goes~~ go down and the output voltage will be brought back down. Besides the ~~mechanism~~ mechanical of this, there is a shortcut correction in the current mode operation. As V_{IN} goes up, the slope of current Ip increases and hence the slope of the ramp of V_{RP} increases. Now the ~~faster~~ steeper ramp equals Verr and the on time (T_{ON}) is shortened. Output voltage changes resulting from input voltage changes will be smaller in amplitude and shorter in duration because of this feedforward characteristic. The output voltage Vo is

$$V_O = V_{IN}\,\frac{Ns}{Np}\,\frac{T_{ON}}{T_{OFF}}$$

By using equation (7), if ~~it~~ Vc = Verr, then ~~we obtain~~

$$T_{ON} = \frac{Verr}{\left(\frac{V_{IN}}{Lp}\bullet Rp + \frac{V_{SL}}{T}\right)} \qquad (9)$$

~~We can find~~ It can be seen that the loop gain of this feedforward characteristic will be reduced by increasing the magnitude of slope compensation V_{SL}/T. Thus, ~~increase~~ increasing the magnitude of slope compensation will decrease the loop gain of the current feedback loop and then reduce the capability of line voltage regulation.

Figures (5) and (6) show two conventional methods of implementing slope compensation. ~~There~~ These methods, however, are unable to solve the problems in the previous description and are unable to operate ~~in~~ under wide input ranges (V_{IN}).

Objects of the Invention

In view of the above advantages and disadvantages with the ~~prior approach,~~ conventional approaches the object of the present invention is to provide a ~~novel~~ solution to ~~avoid~~ these disadvantages and achieve a ~~wide input ranges~~ power ~~conversion. Besides,~~ the objects of the present invention are :

(a) to improve the power conversion efficiency and save ~~the~~ energy.
(b) to shrink the volume of power converter and save the material cost.

These objects are realized in a novel slope compensation construction which allows the power converter to operate in continuous mode under the medium load or heavy load condition. ~~And~~ Furthermore, no minimum load ~~, no~~ or dummy load is required under the light load or no load conditions. The adaptive function of the present invention ~~which will~~ enhances the linearity of the control loop in response to a lower input voltage and permits a higher duty cycle (T_{ON} / T_{OFF}), thereby necessitating only ~~a~~ smaller input capacitor ~~is only need.~~ In an off-line power

~~converters, this~~ converter, a high voltage, high capacity electrolytic capacitor ~~are~~ is expensive and large. It is much more compact and cost effective to use a smaller input capacitor.

Summary of the Invention

In accordance with the present invention, a programmable current source comprises a capacitor, generating a slope ~~signal,~~ signal. This slope signal is added to a current feedback loop for slope compensation~~, the~~. The slope signal is synchronized with the switching signal of power converter via ~~the~~ connection ~~of~~ to a diode; the input of the programmable current source having a resistor, coupled to the voltage feedback loop of the power converter, and generating a slope signal in response to the input voltage and output load of power converter. ~~wherein the~~ The slew rate and magnitude of the slope signal is responsive to the input voltage and output load, and the signal width of the slope signal is equal to the pulse width of the switching signal of power converter.

~~**The Drawing**~~ Brief Description of the Drawings

Fig. (1) is a simplified circuit illustrating a conventional current mode power converter;
Fig. (2) shows ~~the~~ continuous mode current waveforms;
Fig. (3) shows the current waveform under relatively high and relatively low V_{IN};
Fig. (4) is the current loop feedback signal, in which the slope compensation signal is added, ~~illustrates the mechanism~~ thus illustrating of a nonlinear deviation in the power control;
Fig. (5) and (6) show, respectively, two forms of prior art circuits;
Fig. (7) is a schematic diagram illustrating a preferred embodiment of the present invention; and
Fig. (8) is the voltage waveform of ripple in the input capacitor.

Detailed Description of Preferred Embodiment

Fig. ~~(1)~~ (7) shows an embodiment of a current mode power converter constructed in accordance with the present invention. PWM controller U_1 is a general control circuit for current mode power conversion. The switching signal Vsw (the output of U_1) drives a switching MOSFET Q_2. A transformer T_M is placed in series with V_{IN} and Q_2 for the power transfer~~,~~. Switching frequency is determined by capacitor C_3 and the oscillator (osc) in U_1. ~~Due to the~~ The *Latch* of U_1 is set by osc and reset by the comparator (Comp) in ~~U_1, the~~ U_1. Thus, the on time starts at the clock pulse of osc and ends when the voltage level of the signal from the current feedback loop **200** equals ~~to~~ the voltage level of a signal from a voltage feedback loop **150**. The voltage feedback loop consists of error amplifier U_3 and optocoupler U_2. The output voltage of power converter, Vo, is sensed and compared to a reference voltage in the error amplifier U_3. The optocoupler U_2 is required for the isolation in an off-line power converter, otherwise the amplified error voltage can be directly fed to the comparator of U_1. Another input to the comparator is the current feedback signal in which the primary current of transformer T_M is sensed by resistor R_p, and ~~it~~ is coupled to U_1 via the low pass filter R_5 and ~~C_5.~~ C_2. Adaptive slope compensator **100** ~~have~~ has a pnp transistor Q_1, and incorporates resistors R_1, R_2, R_3 to form a programmable current source. Power is supplied from V_R of U_1, ~~it is~~ as a constant voltage (reference voltage) output of U_1. The output of the programmable current source, the collector of Q_1, has a capacitor C_T connected

to ground, which serves to produce a slope waveform, and provides the time constant for the slew rate of the slope signal. A diode D_T is connected between the output of the programmable current source and the output of $U_1(Vsw)$, which serves to synchronize the slope signal **250** with the switching signal Vsw, **300**. ~~Bridge by~~ Bridged the series of D_1 and R4, slope signal **250** is added to the current loop **200** . Via resistor R_1, the input of the programmable current source is connected to any suitable means, exemplified here ~~to~~ as V_{FB}, a voltage feedback loop signal, and thereby the output current of the programmable current source is effected by input voltage V_{IN} and output the power P_O of power converter.

Operation

The operation of the device of Fig (7) in accordance with the invention is as follows :
During the on time (T_{ON}), the switching signal Vsw is high and diode D_T is off, capacitor C_T is charged by the programmable current source. Mathematically this can be stated as

$$V_{SL}=\frac{I_{R3}\cdot\Delta T}{C_T}$$

~~if~~ If the gain (h_{FE}) of Q1 is ~~enough~~ high enough, then

$$I_{R3}=(V_{R2}-V_{EB(Q1)})\,/\,R_3$$

$$V_{R2}=(V_R-V_{FB})\ \bullet[R_2/(R_1+R_2)]$$

The equation can be written as

$$V_{SL}=\frac{\Delta T}{R3.C_T}[(V_R-V_{FB})\ \bullet\frac{R2}{R1+R2}-V_{EB(Q1)}] \qquad (10)$$

$$\frac{\partial V_{SL}}{\partial V_{FB}}=\frac{-R2}{R3(R1+R2)C_T}.\Delta T \qquad (11)$$

Since the change of V_{FB} is ~~direct proportion~~ directly proportional to the change of V_{IN} and ~~inverse proportion~~ inversely proportional to the change of output power P_O, $\Delta V_{FB}=+K_1\Delta V_{IN}-K_2\Delta P_O$, where K_1, K_2 are loop gain ~~constant~~ constants of the voltage feedback loop. Thus, the equation (11) can be stated as :

$$\Delta V_{SL}=\frac{R2}{R3(R1+R2)C_T}\Delta T\ .\ (-K_1\Delta V_{IN}+K_2\Delta P_O) \qquad (12)$$

During the off time (T_{OFF}), the switching signal Vsw is low, diode D_T is on, capacitor C_T is discharged and the slope signal is reset to zero. Since the slope signal is synchronized with the switching signal, the rising time ΔT of slope signal is equal to the on time T_{ON}. ~~thus~~ Thus equations (10) and (12) can be written as :

$$V_{SL}=\frac{T_{ON}}{R3C_T}\ [(V_R-V_{FB}).\ \frac{R2}{R1+R2}-V_{EB(Q1)})] \qquad (13)$$

$$\Delta V_{SL}=(\frac{R2}{R1+R2})\frac{T_{ON}}{R3C_T}.(-K_1\Delta V_{IN}+K_2\Delta P_O) \qquad (14)$$

In one specific implementation of the Fig. (7) arrangement, a 50W (P_O: $20V_{DC}/2.5A$) off-line power converter, the input voltage is rated $90V_{AC}\sim 265V_{AC}$ RMS, using a small input capacitor C_{IN} as 68 uF (microfarad), 400 volt electrolytic device. An EFD-30 ferrite core was used, operating in continuous mode under the medium load and full load. ~~The~~ An efficiency of 85% ~ 88% was obtained responding to the change of V_{IN} ($90V_{AC}\sim 265V_{AC}$). ~~And~~ Furthermore, less than 2W was consumed under the no load condition. According to the principle of equations (13), (14) and the measurement in the implementation, the following results ~~are~~ were observed :